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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,727	10/22/2003	Andrew Harvey Barr	200310431-1	7682

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EXAMINER	
ASSESSOR, BRIAN J	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 09/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/690,727	BARR ET AL.	
	Examiner	Art Unit	
	Brian J. Assessor	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☒ Claim(s) *19 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/22/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 14 recites the limitation "selected execution unit". There is insufficient antecedent basis for this limitation in the claim.

Claim 18 recites the limitation "circuitry" in which circuitry being referred to is not known. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 13 and 14 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Claims 13 and 14 are program product claims, which are effectively programs, which are not statutory under 35 USC 101.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 13 and 15-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Quach (6,625,749).

As per claim 13, Quach teaches:

A computer-readable program product for execution on a target microprocessor having multiple CPU cores integrated thereon, the program product comprising:

diagnostic code configured to be executed on a selected CPU core; (Quach column 3, lines 47-49)

program code configured to be executed on remaining CPU cores. (Quach column 3, lines 44-49)

As per claim 15, Quach teaches:

A microprocessor comprising:

a plurality of CPU cores integrated on the microprocessor chip; (Quach figure 1, elements 110(a) and 110(b))

inter-core communications circuitry coupled to each of the CPU cores and configured to perform context switching between the CPU cores. (Quach column 5, lines 13-17)

As per claim 16, Quach teaches:

The microprocessor of claim 15, wherein each CPU core comprises a processor core and an associated local cache memory. (Quach column 4, lines 55-57; a cache would be required to execute these processes)

As per claim 17, Quach teaches:

The microprocessor of claim 15, further comprising:

control circuitry coupled to the inter-core communications circuitry and configured select a first CPU core currently in use for diagnostic testing. (Quach column 12, lines 21-24)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 6, and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach (6,625,749) in view of Haroun (20040168105).

As per claim 1:

A method of executing program code on a target microprocessor with multiple CPU cores thereon, the method comprising:

performing inter-core context switching; executing in parallel (Quach column 4, lines 55-57)

diagnostic code on the selected CPU core and the program code on remaining CPU cores. (Quach column 3, lines 44-49; there are two independent operations occurring in parallel.)

Quach does not explicitly disclose a method for selecting one of the CPU cores for testing. On page 3, paragraph 0032 Haroun clearly teaches a method for testing CPU cores one at a time and selecting the core to be tested.

It would have been obvious to a person of ordinary skill in the art at the time of invention to include the method as taught by Haroun in order to allow for improved core testing. This would have been obvious because Haroun clearly teaches that the above method is better suited for testing individual cores without a complex system. (Haroun page 2, paragraph 13)

As per claim 4:

The method of claim 1, further comprising:

setting a level of aggressiveness for scheduling the testing of the execution units. (Quach column 3, lines 54-56; aggressiveness - anytime a soft error occurs the testing is started.)

As per claim 6:

The method of claim 1, wherein the multiple CPU cores comprise at least four CPU cores integrated onto the microprocessor integrated circuit. (Haroun figure 1)

As per claim 7:

The method of claim 1, wherein the multiple CPU cores comprise at least eight CPU cores integrated onto the microprocessor integrated circuit. (Haroun figure 1; inherent; a method done with 4 CPU cores could be done with 8.)

Claim 2, 3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach (6,625,749) in view of Haroun (20040168105) in further view of Quach (6,640,313 herein refered to as Quach II).

As per claim 2:

Quach and Haroun do not explicitly disclose a method wherein the selection of the CPU core for testing utilizes an algorithm that assures testing of each of the multiple CPU cores.

In column 10, lines 5-13, Quach II clearly discloses a method for selection of CPU cores for testing utilizes an algorithm that assures testing of the CPU cores. It would have been obvious to a person of ordinary skill in the art at the time of invention to include the method as taught by Quach II in order to make an organized testing method. This would have been obvious because Quach II clearly teaches that the above method is better suited for reliability in computer systems using core processing. (Quach II column 2, lines 15-25)

As per claim 3:

The method of claim 2, wherein the algorithm comprises a round-robin type algorithm. (Quach II, inherent; round robin is a well known algorithm in testing multiple devices.)

As per claim 5:

The method of claim 4, further comprising:

applying an aggressiveness-dependent algorithm to determine when to schedule all available cores for execution of the program code and when to schedule parallel execution of the program code and the diagnostic code. (Quach column 10, lines 26-29)

Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach (6,625,749) in view of Haroun (20040168105) in further view of Raina (6,134,675).

As per claim 8:

Quach and Haroun do not explicitly disclose a method wherein the diagnostic code performs diagnostic operations from a test pattern comprising operations with known expected results.

In column 3, line 19-22 Raina clearly discloses a method for using diagnostic code to perform diagnostic operations on CPU cores from a test pattern with known expected results. It would have been obvious to a person of ordinary skill in the art at the time of invention to include the method as taught by Raina in order to make a more

thorough core testing method. This would have been obvious because Raina clearly teaches that the above method is better suited for testing integrated circuits containing multiple cores. (Raina column 1, lines 22-23)

As per claim 9:

The method of claim 8, wherein the diagnostic code compares an actual result with a known expected result. (Raina column 3, line 19-22)

As per claim 10:

The method of claim 9, wherein the diagnostic code jumps to a fault handler if the compared results are different. (Raina column 3, line 14-22)

As per claim 11:

The method of claim 10, wherein the fault handler includes code to remove a faulty CPU core from use in executing the program code. (Raina column 3, line 17-19)

As per claim 12:

The method of claim 10, wherein the fault handler includes code to perform a system halt to prevent data corruption. (Raina column 3, line 17-19)

Allowable Subject Matter

Claims 19 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian J. Assessor whose telephone number is (571) 272-0825. The examiner can normally be reached on M-F 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

BA

SCOTT BADERMAN
SUPERVISORY PATENT EXAMINER